In the Claims:

1. (Original) A method for forming an electronic device, the method comprising:

forming a capacitor structure on a portion of a substrate, the capacitor structure including a first electrode on the substrate, a capacitor dielectric on the first electrode, a second electrode on the dielectric, and a hard mask on the second electrode so that the capacitor dielectric is between the first and second electrodes, so that the first electrode and the capacitor dielectric are between the second electrode and the substrate, and so that the first and second electrodes and the capacitor dielectric are between the hard mask and the substrate;

forming an interlayer dielectric layer on the hard mask and on portions of the substrate surrounding the capacitor structure;

removing portions of the interlayer dielectric layer to expose the hard mask while maintaining portions of the interlayer dielectric layer on portions of the substrate surrounding the capacitor structure; and

removing the hard mask thereby exposing portions of the second electrode while maintaining the portions of the interlayer dielectric layer on portions of the substrate surrounding the capacitor.

2.(Original) A method according to Claim 1 further comprising:

after removing the hard mask layer, forming a plate line on the exposed portions of the second electrode.

3. (Original) A method according to Claim 1 wherein the capacitor dielectric comprises a ferroelectric material.

4. (Original) A method according to Claim 3 wherein the ferroelectric material comprises a material selected from the group consisting of PZT, SBT, and/or BLT.

5. (Original) A method according to Claim 1 wherein removing portions of the interlayer dielectric layer comprises planarizing the interlayer dielectric layer to a level of the hard mask.

6. (Original) A method according to Claim 5 wherein planarizing the interlayer dielectric layer comprises at least one of chemical mechanical polishing and/or an etching back.

7. (Original) A method according to Claim 1 wherein the interlayer dielectric layer, the hard mask, and the second electrode comprise different materials.

8. (Original) A method according to Claim 7 wherein removing the hard mask comprises etching the hard mask using an etchant that selectively etches the hard mask with respect to the interlayer dielectric layer and the second electrode.

9. (Original) A method according to Claim 8 wherein the etchant comprises phosphoric acid.

10. (Original) A method according to Claim 7 wherein the hard mask comprises a layer of at least one material selected from the group consisting of silicon nitride and/or titanium nitride.

11. (Original) A method according to Claim 1 wherein forming the capacitor structure comprises:

forming a first electrode layer on the substrate;

forming a dielectric layer on the lower electrode layer opposite the substrate;

forming a second electrode layer on the dielectric layer opposite the first electrode and the substrate;

forming a hard mask layer on the second electrode layer opposite the dielectric layer, the first electrode layer, and the substrate;

patterning the hard mask layer to provide the hard mask on the second electrode layer; and

etching portions of the second electrode layer, the dielectric layer, and the first electrode layer using the hard mask as an etching mask to provide the first electrode, the capacitor dielectric, and the second electrode.

12.(Original) A method according to Claim 1 wherein each of the first and second electrodes comprises at least one material selected from the group consisting of ruthenium (Ru), platinum (Pt), iridium (Ir), rhodium (Rh), osmium (Os), and/or oxides thereof.

13. (Original) A method according to Claim 1 wherein the hard mask has a thickness in the range of approximately 50 nanometers to 200 nanometers.

14. (Original) A method according to Claim 1 wherein a thickness of the hard mask is greater than a variation in thickness of the portions of the interlayer dielectric layer maintained on portions of the substrate surrounding the capacitor structure after removing portions of the interlayer dielectric layer.

15. (Original) A method according to Claim 1 wherein the interlayer dielectric layer comprises silicon oxide.

16. (Original) A method according to Claim 1 further comprising:

prior to forming the interlayer dielectric layer, forming a hydrogen barrier layer on the capacitor structure including the hard mask, the first and second electrodes, and the capacitor dielectric.

17. (Original) A method according to Claim 16 wherein the hydrogen barrier layer comprises a material selected from the group consisting of titanium oxide (TiO_2), aluminum oxide (Al_2O_3), zirconium oxide (ZrO_2), and cerium oxide (CeO_2).

18. (Original) A method according to Claim 1 further comprising:

prior to forming the capacitor structure, forming a memory cell access transistor wherein the first electrode of the capacitor structure is electrically connected to a source/drain region of the memory cell access transistor.

19. (Currently Amended) A method according to Claim [[1]] 18 further comprising:

prior to forming the capacitor structure, forming an insulating layer on the memory cell access transistor, the insulating layer including a via therein exposing a portion of the source/drain region of the memory cell access transistor, and the first electrode being electrically connected to the source/drain region through the via.

20. (Original) A method of fabricating a ferroelectric memory device, comprising:

forming a lower interlayer dielectric on a semiconductor substrate;

sequentially stacking a ferroelectric capacitor and a hard mask pattern on the lower interlayer dielectric;

forming an inter-metal dielectric to cover an entire surface of a semiconductor substrate including the hard mask pattern;

planarizing the inter-metal dielectric to expose the hard mask pattern;

selectively removing the exposed hard mask pattern to expose a top surface of the ferroelectric capacitor; and

forming a plate line contacting with the top surface of the ferroelectric capacitor.

21. (Original) The method as set forth in claim 20, wherein the hard mask pattern is made of a material having an etch selectivity with respect to the inter-metal dielectric.

22. (Original) The method as set forth in claim 20, wherein the hard mask pattern is made of silicon nitride or silicon nitride and titanium nitride which are sequentially stacked.

23. (Original) The method as set forth in claim 20, wherein the formation of the ferroelectric capacitor and the hard mask pattern comprises:

sequentially stacking a lower electrode layer, a ferroelectric layer, an upper electrode layer, and a hard mask layer on the lower interlayer dielectric;

patterning the hard mask layer to form a hard mask pattern; and

using the hard mask pattern as a mask, successively patterning the upper electrode layer, the ferroelectric layer, and the lower electrode layer to sequentially form a lower electrode, a ferroelectric pattern, and an upper electrode.

24. (Original) The method as set forth in claim 23, wherein the lower electrode layer and the upper electrode layer are made of at least one selected from the group consisting of ruthenium (Ru), platinum (Pt), iridium (Ir), rhodium (Rh), osmium (Os), and oxide thereof.

25. (Original) The method as set forth in claim 23, wherein the ferroelectric layer is made of one selected from the group consisting of PZT, SBT, and BLT.

26. (Original) The method as set forth in claim 20, wherein the planarization of the inter-metal dielectric is done by a chemical mechanical polishing (CMP) process or an etch-back process.

27. (Original) The method as set forth in claim 20, wherein the selective removal of the hard mask pattern is done using an etch recipe having an etch selectivity with respect to the inter-metal dielectric and the ferroelectric capacitor.

28. (Original) The method as set forth in claim 20, wherein the selective removal of the hard mask pattern is done using an etchant containing phosphoric acid.

29. (Original) The method as set forth in claim 20, wherein the hard mask pattern has a thickness ranging from 50 nanometers to 200 nanometers.

30. (Original) The method as set forth in claim 20, wherein a thickness of the hard mask pattern is greater than a maximum thickness deviation based on the planarization of the inter-metal dielectric.

31. (Original) The method as set forth in claim 20, wherein the inter-metal dielectric is made of silicon oxide.

32. (Original) The method as set forth in claim 20, prior to formation of the inter-metal dielectric, further comprising forming a hydrogen barrier layer to cover a sidewall of the ferroelectric.

33.(Original) The method as set forth in claim 32, wherein the hydrogen barrier layer is made of at least one selected from the group consisting of titanium oxide (TiO_2), aluminum oxide (Al_2O_3), zirconium oxide (ZrO_2), and cerium oxide (CeO_2).